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Attorney Docket No. 5646-113 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Declan McDonagh et al. Group Art Unit: 2816
Serial No.: 10/648,090 Confirmation No.: 2780
Filed: August 26, 2003
For: CLOCK SIGNAL GENERATORS HAVING PROGRAMMABLE FULL-PERIOD CLOCK SKEW CONTROL AND METHODS OF GENERATING CLOCK SIGNALS HAVING PROGRAMMABLE SKEWS

Date: August 11, 2004

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on Form PTO-1449, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the waiver by the U.S. Patent and Trademark Office of requirements under 37 C.F.R. § 1.98(a)(2)(i) for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003.

It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 11, 2004.

Candi L. Riggs

Candi L. Riggs

FORM PTO-1449 U.S. Department of Commerce
Patent and Trademark Office

LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

Attorney Docket Number	Serial No.
5646-113	10/648,090
Applicants: Declan McDonagh et al.	
Filing Date: August 26, 2003	Group 2816

U. S. PATENTS & PATENT APPLICATION PUBLICATIONS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	6,539,072	03-25-03	Donnelly et al.	375	371	
	2	6,125,157	09-26-00	Donnelly et al.	375	371	
	3	5,614,855	03-25-97	Lee et al.	327	158	
	4	5,485,490	5,485,490	Leung et al.	375	371	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes | No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	5	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496

EXAMINER _____ DATE CONSIDERED

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.